



RS780LQ-CM V1.0

09/7/23

SCHEMATICS TABLE:

Page	Index	Page	Index
1	COVER PAGE	17	SB710-STRAPS
2	BLOCK DIAGRAM	18	CRT(D-sub)-VGA
3	HT,CPU MEMORY	19	PCIE-16X/1X SLOT
4	CPU CONTROL & MISC	20	TPM, USB, 5VDUAL SWITCH
5	CPU PWR & GND	21	PCI SLOT
6	DDR3 DIMM	22	SIO IT8720-PS2/FDD/CIR
7	RS740/RS780-HT LINK I/F	23	LPT/COM PORT
8	RS740/RS780-PCIE I/F	24	LAN 8103EL/8102EL/8111DL
9	RS740/RS780-SYSTEM I/F	25	AUDIO ALC662/ALC888
10	RS740/RS780-SPMEM/STRAPS	26	ALC662/ALC888(PANEL)
11	RS740/RS780-POWER	27	ISL6323B VCORE VOLTAGE
12	CLOCK GENERATOR-ICS9LPRS471	28	DC POWER, DDRIII POWER
13	SB710-PCIE/PCI/CPU/LPC/CLK	29	NB CORE POWER
14	SB710-ACPI/GPIO/USB/AUDIO	30	PANEL,ATX24P,SMRT FAN,BUZZER
15	SB710-POWER & DECOUPLING	31	POWER ENABLE
16	SB710-SATA/IDE/HWM/SPI	32	Attention

*Reference Document:

42336_rs780_dg_nda_2.00

43303_sb700_dg_nda_1.05

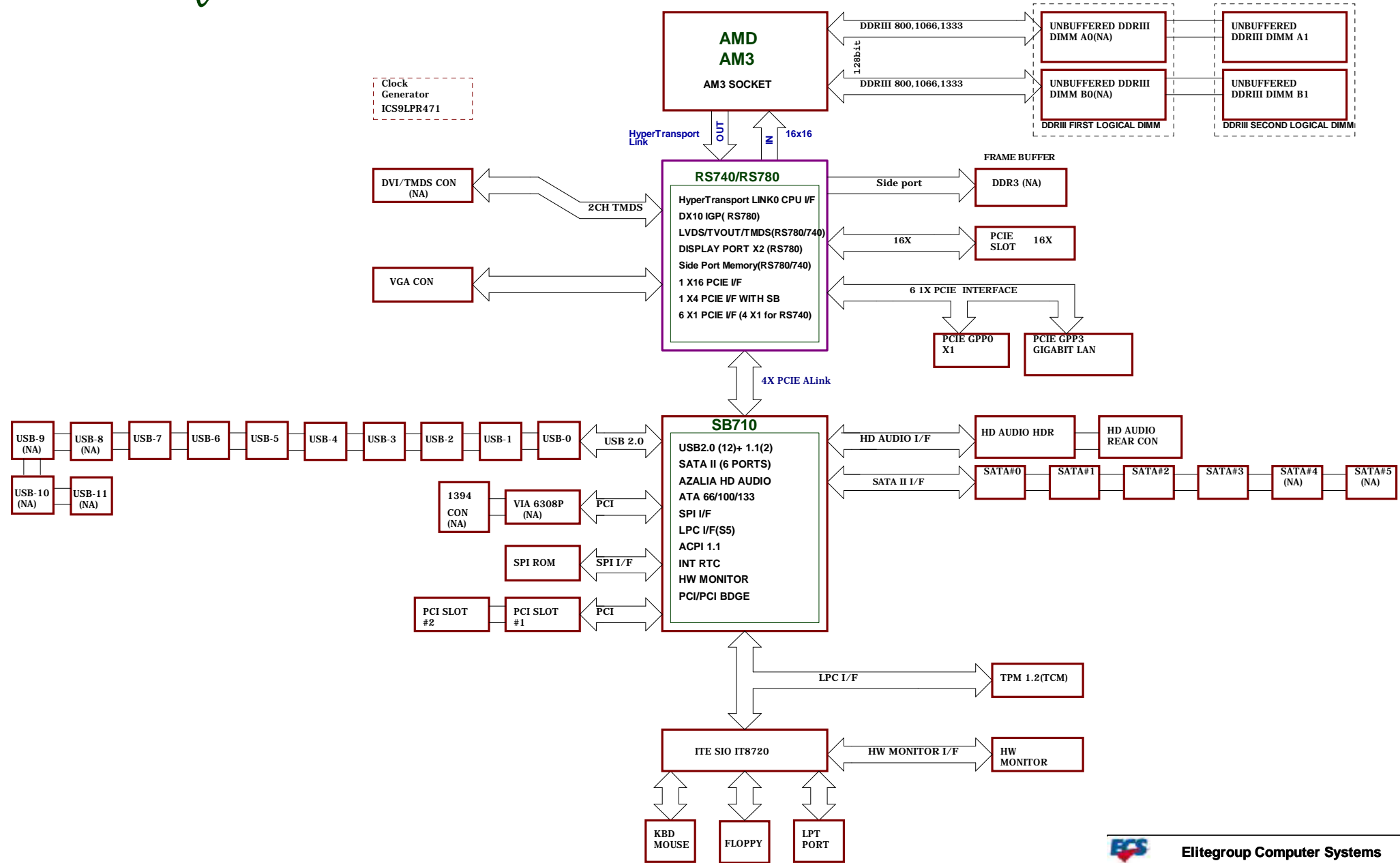
PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

REVISION HISTORY:

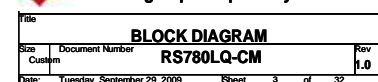
Rev	Date	Notes
V.A	2009.7.22	First release
V1.0	2009.8.14	P20, Modify GP40 pull-high to fix S3 issue P29, Modify U20 VDDA circuit P30, Modify Buzzer circuit
	2009.9.14	P09, Reserve the gate circuit to prevent from the glitch



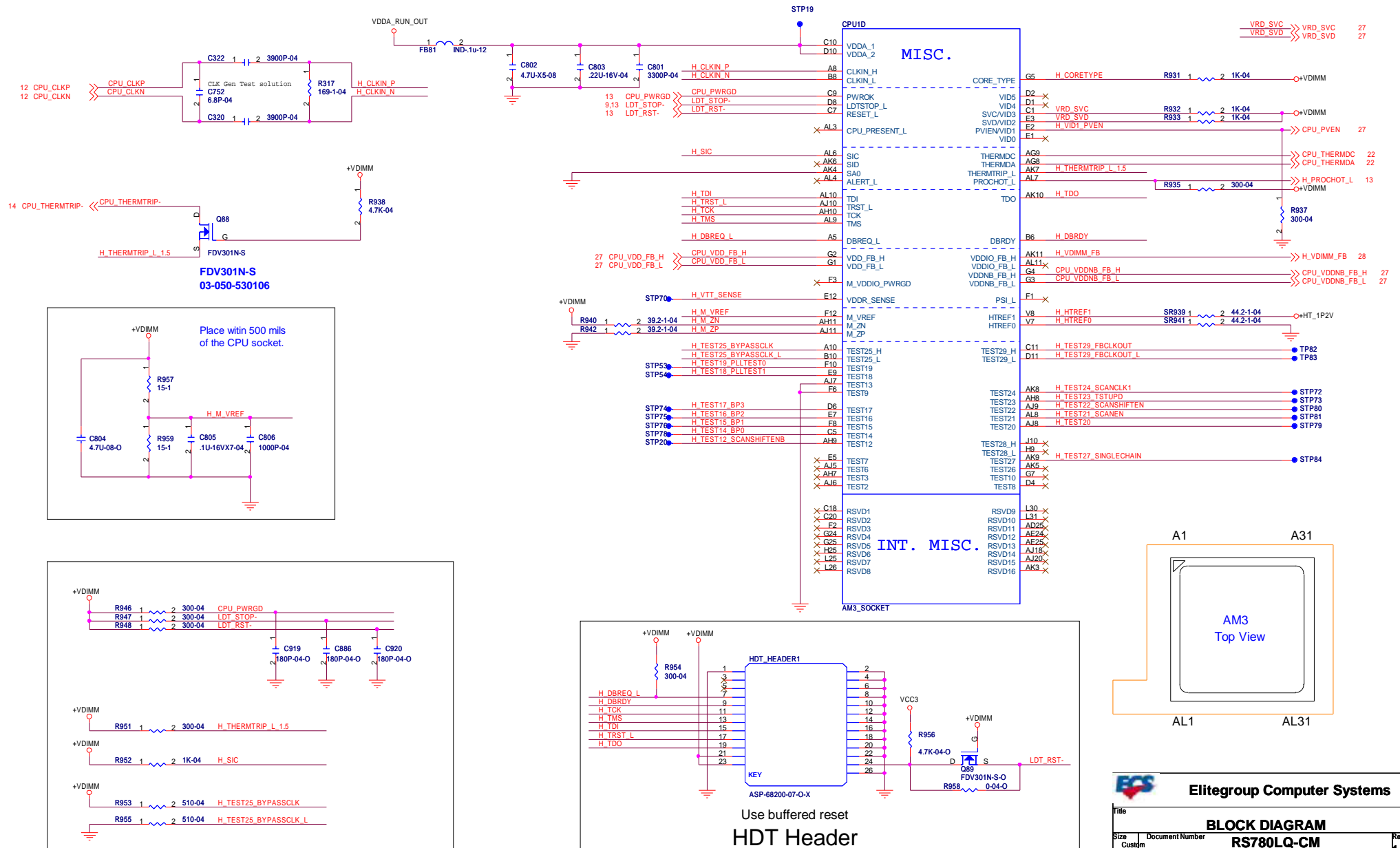
RS780LQ-CM



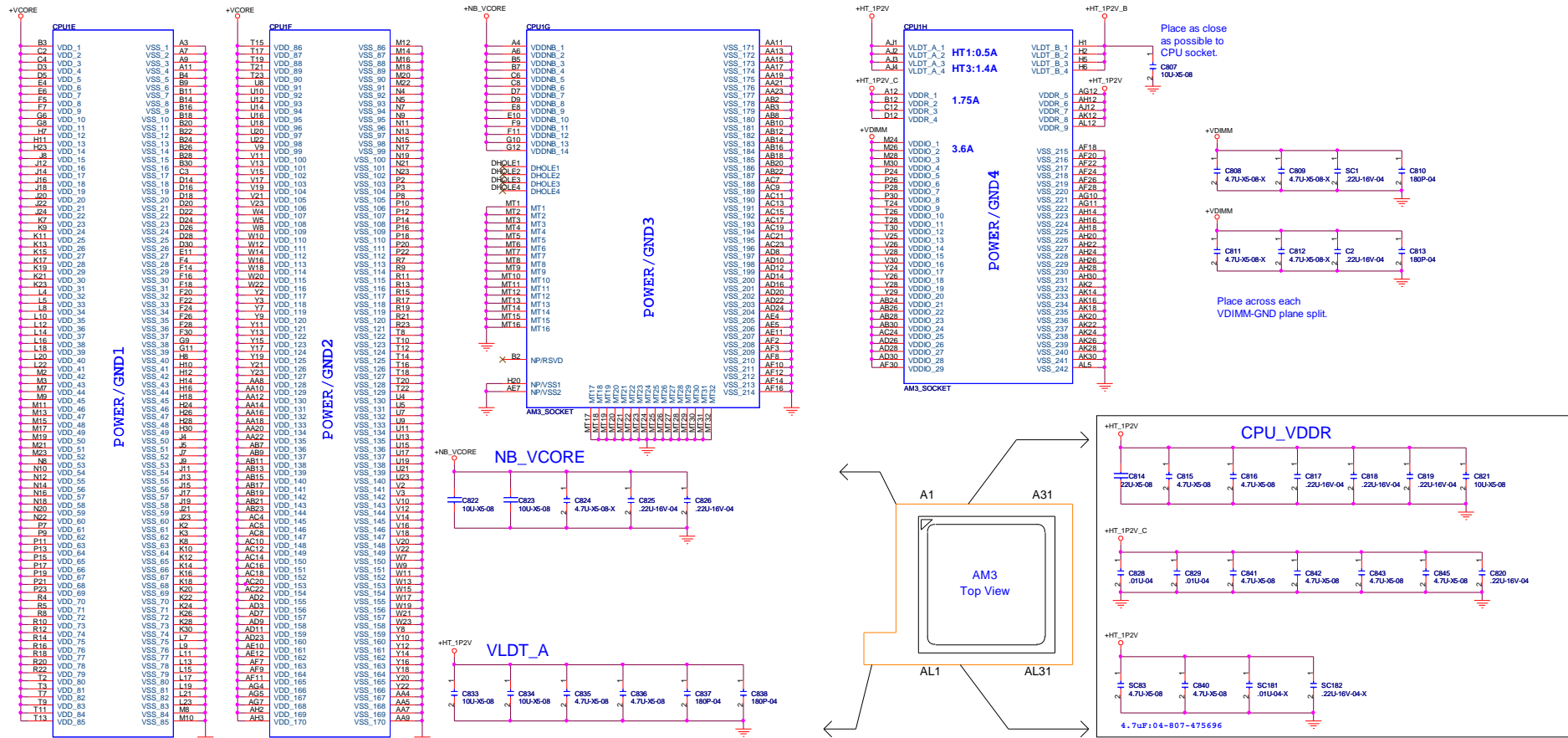
HT LINK



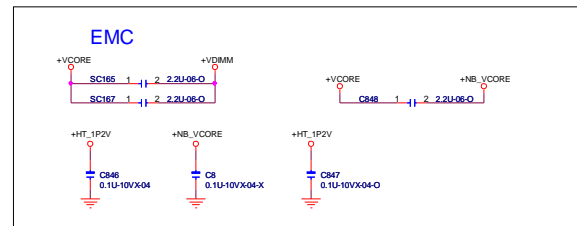
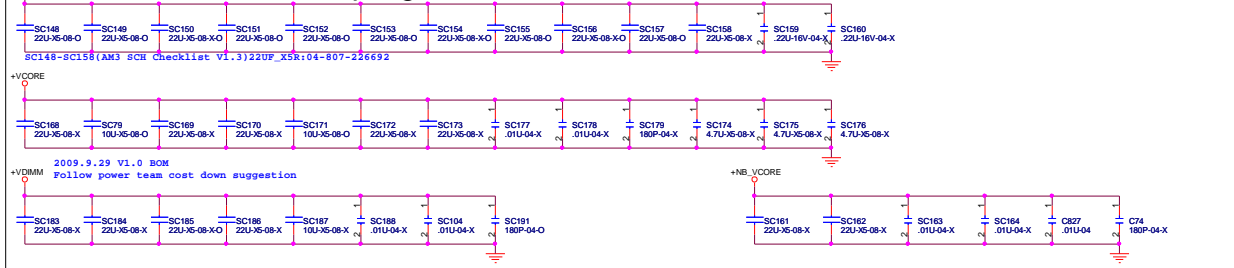
CPU Control and Miscellaneous

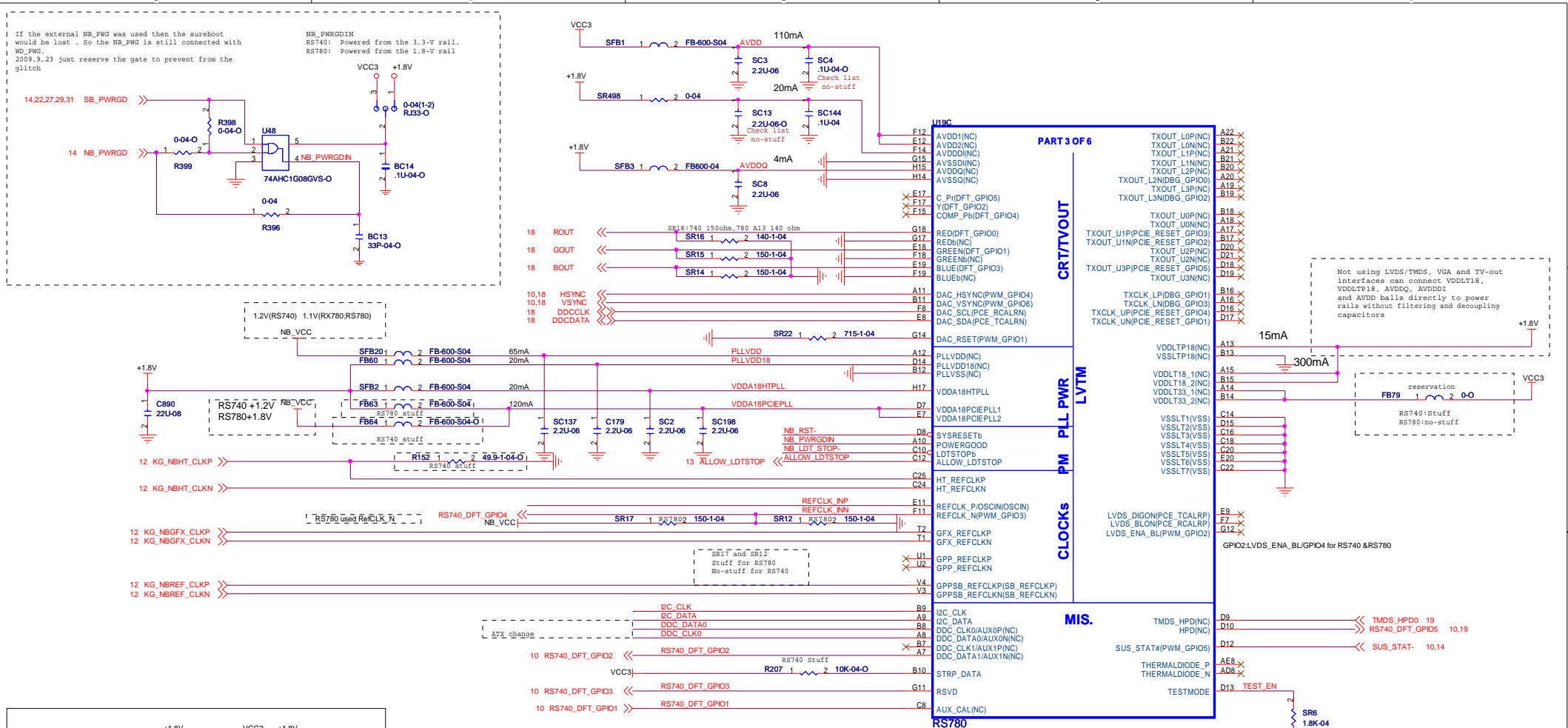


Processor Power and Ground



Bottom Side Decoupling





RS740/RS780/RS780LQ-CM

Elitegroup Computer Systems

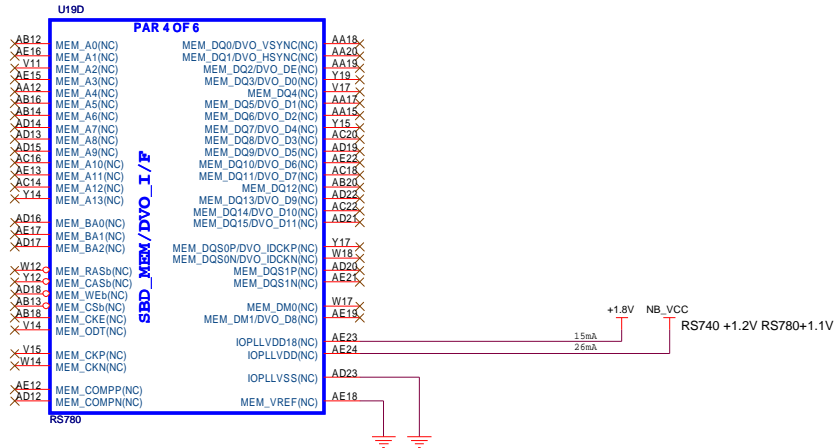
Rev 1.0

Document Number: **RS740/RS780-SYSTEM I/F**

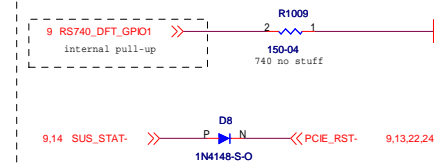
Rev: **1.0**

Date: Tuesday, September 29, 2009

Sheet: 9 of 32

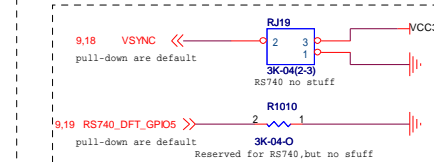


RS740/RS780 STRAPS



RS740/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS740: pin DFT_GPIO1
 RX780: pin DFT_GPIO1
 RS780: pin SUS_STAT#

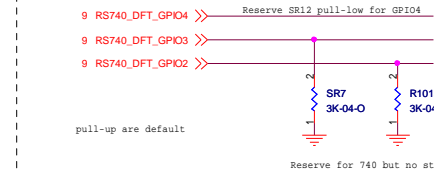


RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO
 1 : Disable (RS740/RS780); Enable (RX780)
 0 : Enable (RS740/RS780); Disable (RX780)
 RS740: pin DFT_GPIO5
 RX780: pin DFT_GPIO5
 RS780: pin VSYNC

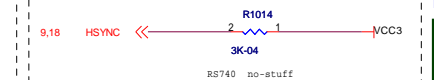
RS780: STRAP_PCIE_GPP_CFG[2:0] (configure thru register setting)

1-1-1-1-1-1	Mode L	default
1-1-1-1-1-1	Mode L	
2-0-2-0-2-0	Mode C2	
2-0-2-0-1-1	Mode K	
2-0-1-1-1-1	Mode E	
1-1-1-1-1-1	Mode L	
4-0-0-0-1-1	Mode C	
4-0-0-0-2-0	Mode B	



RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

These pin straps are used to configure PCI-E GPP mode.
 111: register defined (register default to Config E) default
 110: 4-0-0-0-0-0 Config A
 101: 4-4-0-0-0-0 Config B
 100: 4-2-2-0-0-0 Config C
 011: 4-2-1-1-0-0 Config D
 010: 4-1-1-1-1-1 Config E
 others: register defined (default to Config E)



RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory
 1. Disable (RS740/RS780)
 0 : Enable (RS740/RS780)
 RS740: pin DFT_GPIO0
 RS780: pin HSYNC
 RX780: Not Applicable

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

Enables Test debug bus using PCIE bus
 1. Disable (can be enabled thru nbcfg register)
 0 : Enable
 RX780: pin DFT_GPIO0
 RS780: configurable thru register setting only
 RS740: Not supported



Elitegroup Computer Systems

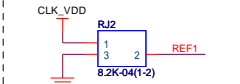
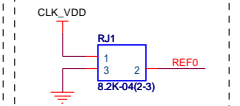
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	ref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF (N/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF (OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will be configured as input mode, BIOS can program it to output mode.

SEL_HTT66:
RS740: Connected to 3.3V_S0 through an 8.2-k Ω 5% resistor to select a 66-MHz single-ended HT clock output. RS780/RX780: Connected to GND through an 8.2-k Ω 5% resistor to select a 100-MHz differential HT clock output.

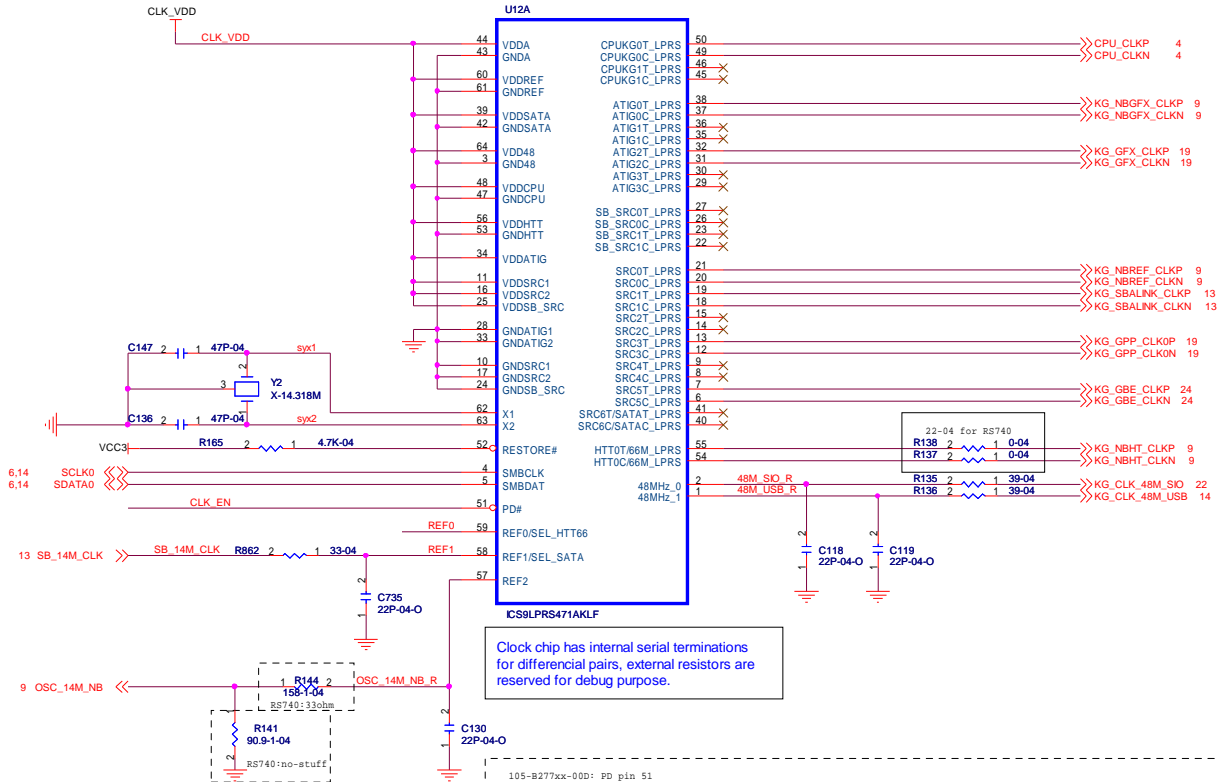
RS780:2-3 stuff
RS740:1-2 stuff



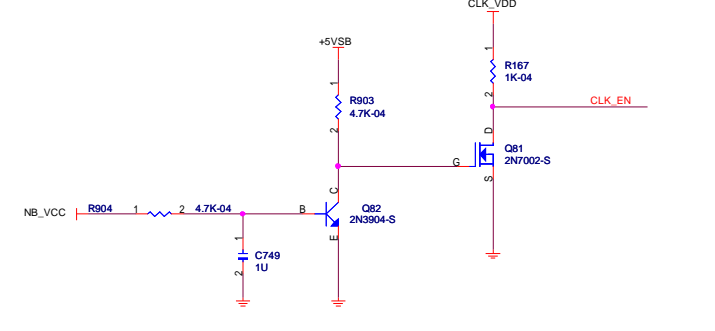
	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

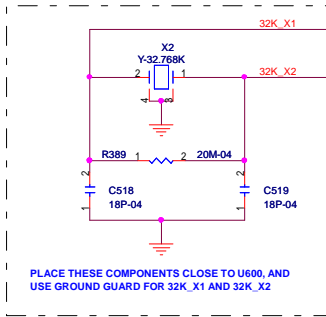
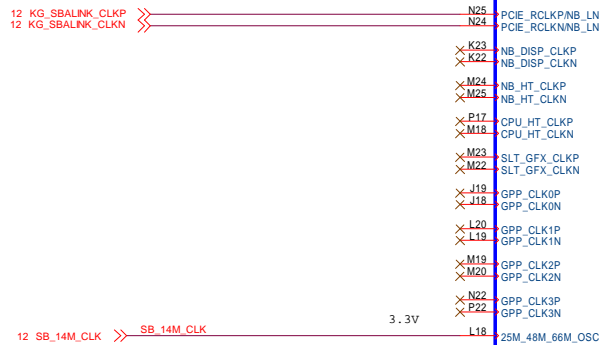
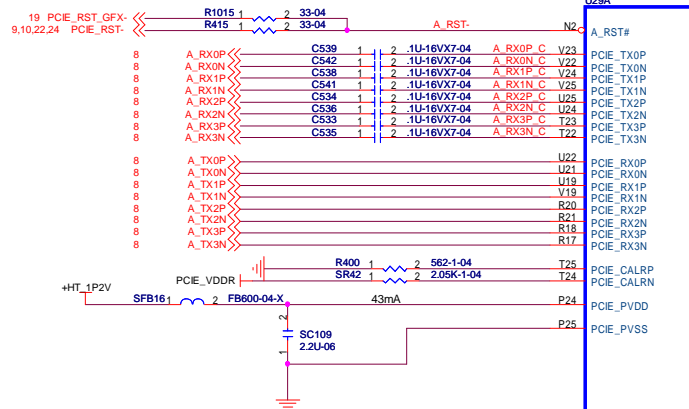
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK



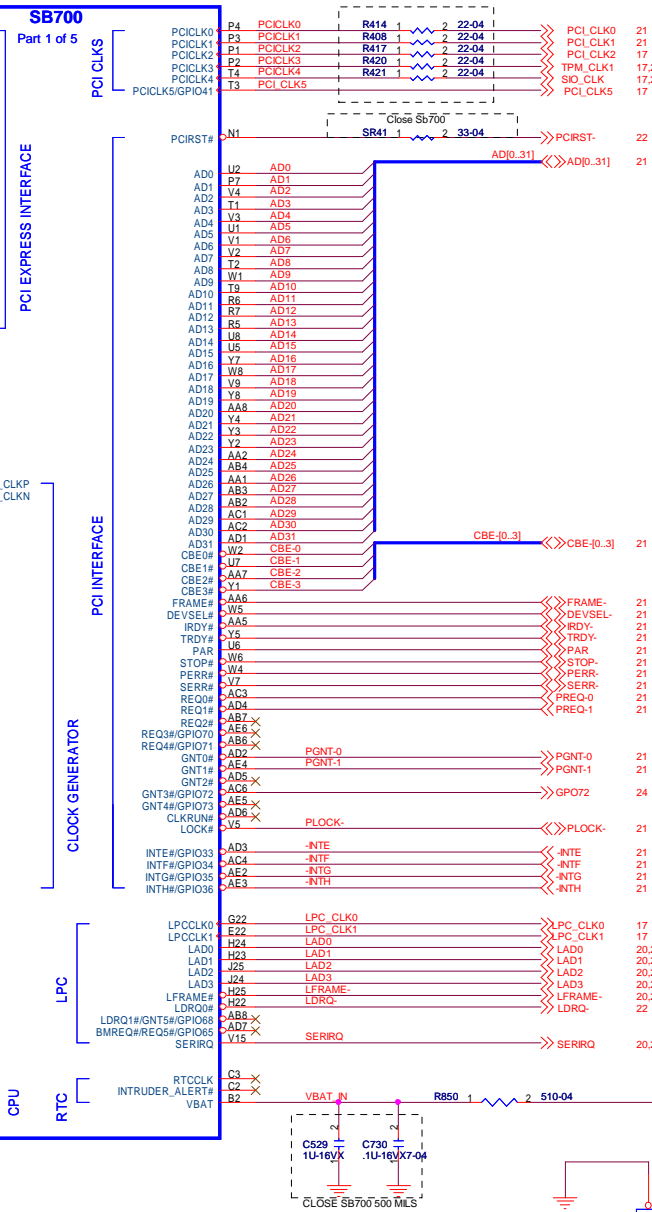
105-B277xx-000: PD pin 51
The SB700 need +1.2V stable before it receive clock
KG_SBALINK_CLKP/N to make sure of that, it is recommended to add +1.2V gating to clock generator

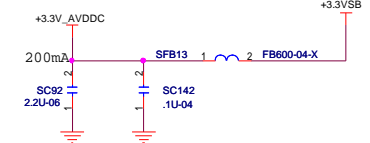




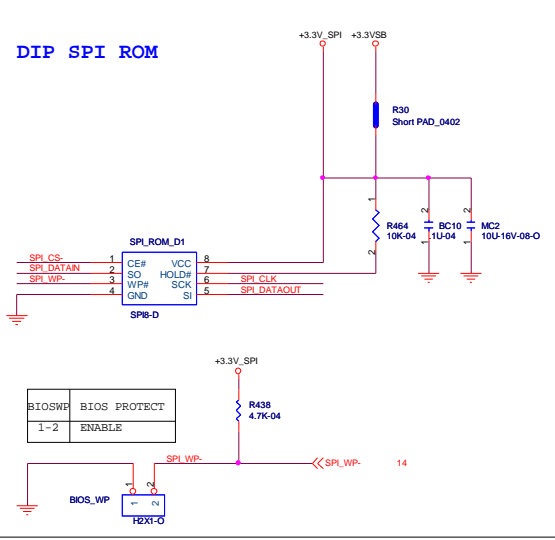
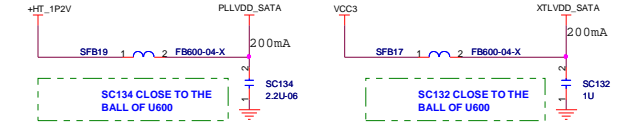
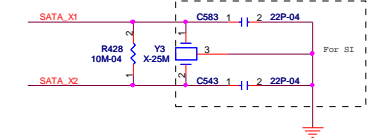
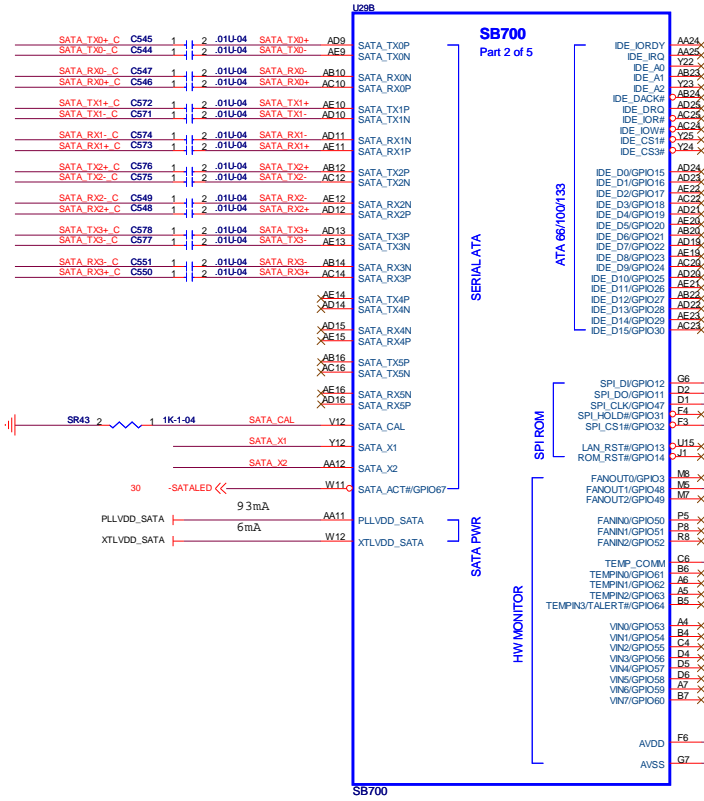
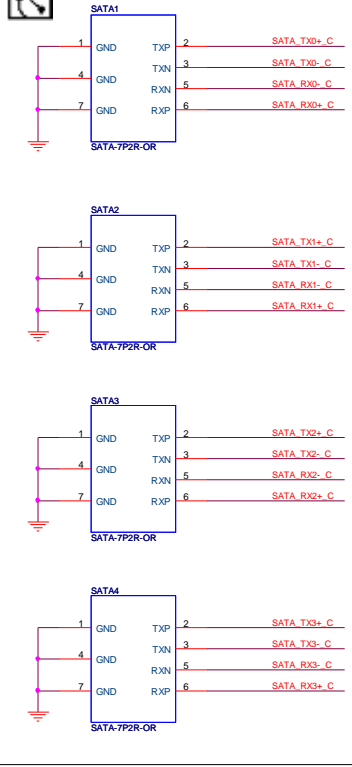
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

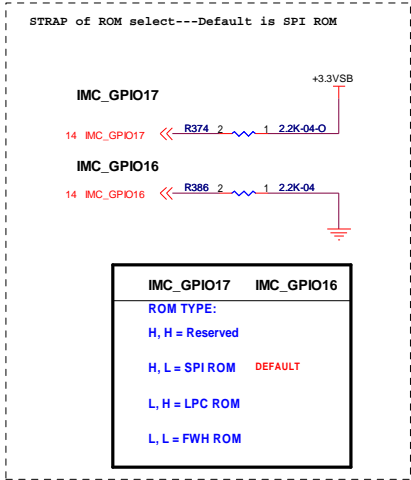
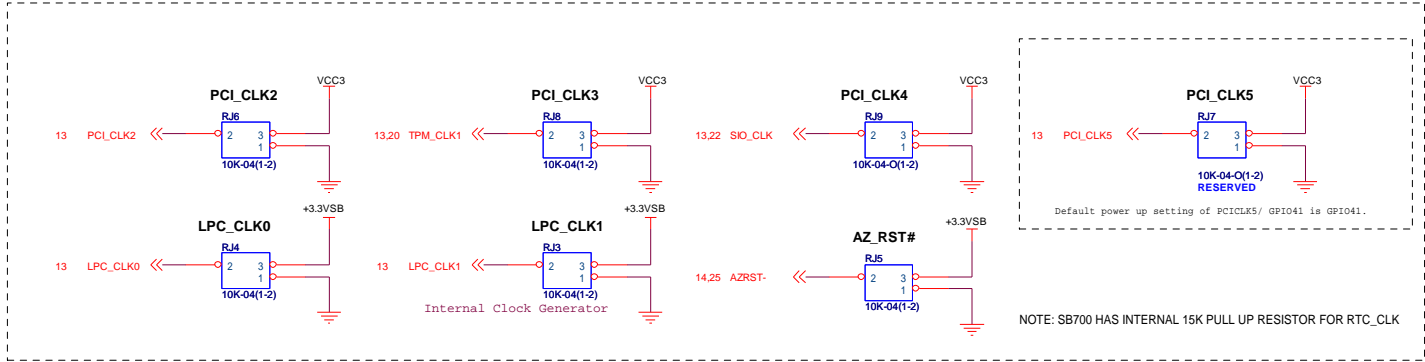
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.





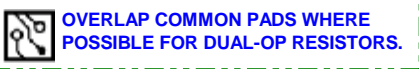
NOTE: J600&J601&J602&J603 ARE THT CONNECTORS





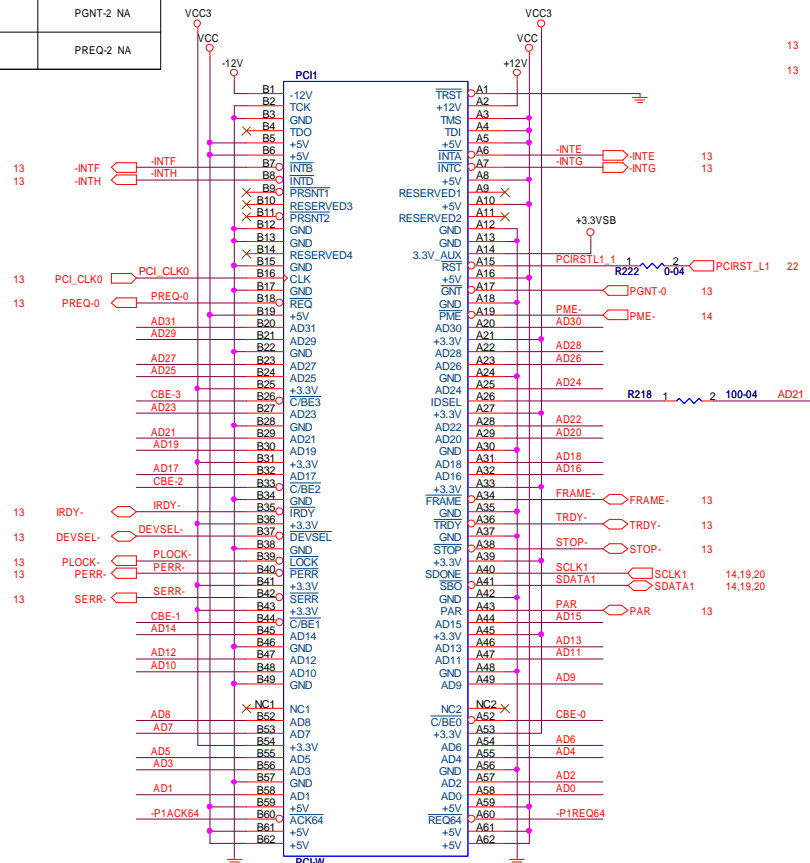
REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	ENABLE PCI MEM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	DISABLE PCI MEM BOOT DEFAULT	L, H = LPC ROM L, L = FWB ROM	

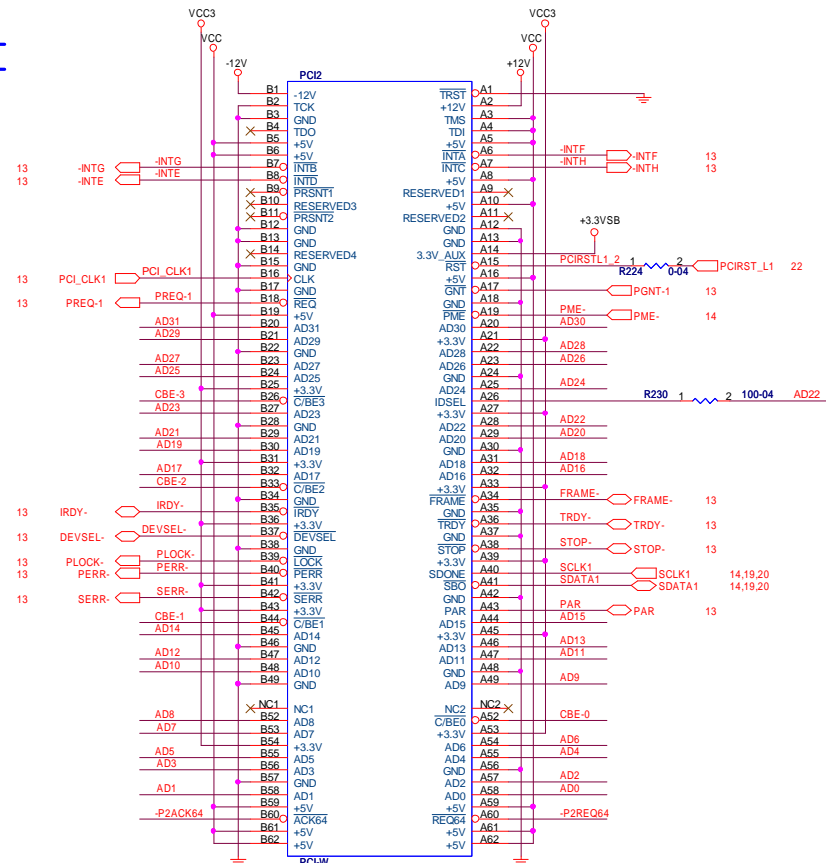


OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

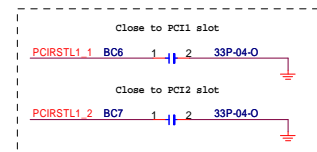
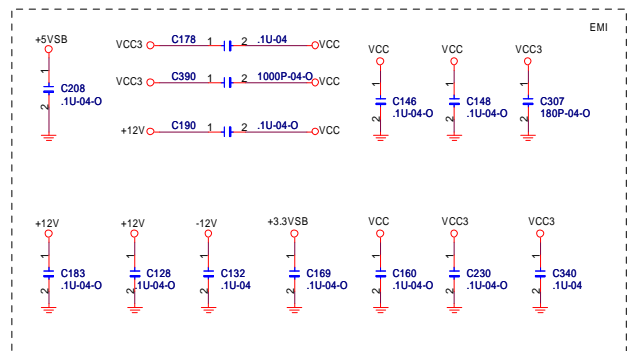
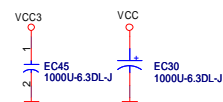
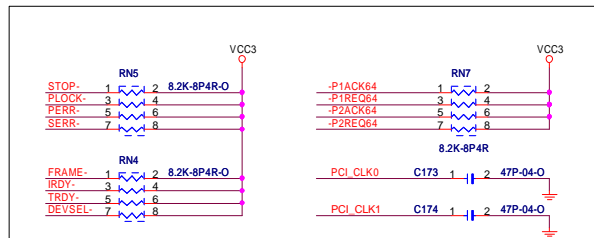
SLOT1	SLOT2	1394 NA
AD21	AD22	AD23 NA
PGNT-0	PGNT-1	PGNT-2 NA
PREQ-0	PREQ-1	PREQ-2 NA



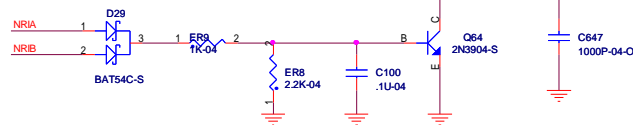
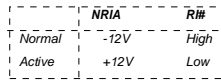
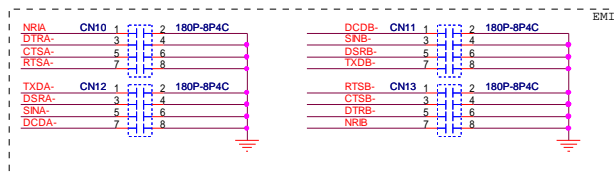
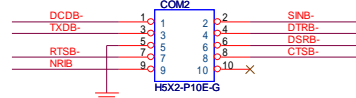
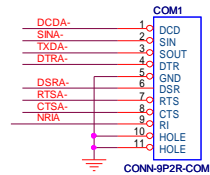
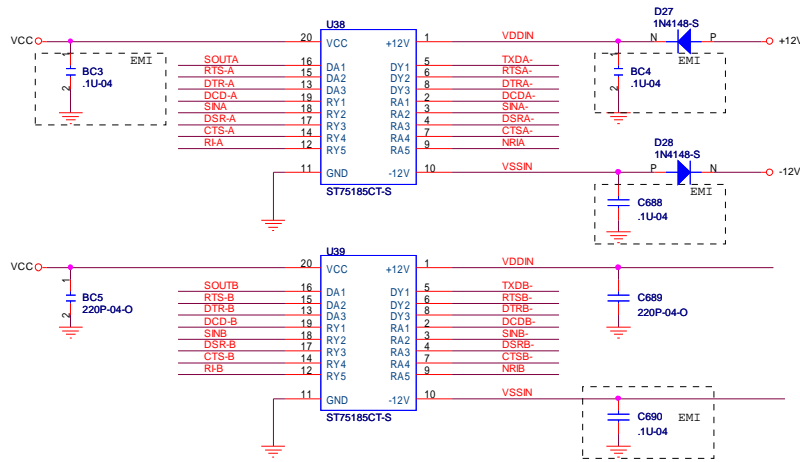
INT:E
IDSEL:AD21



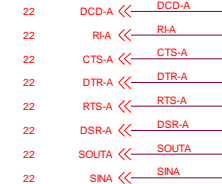
INT:F
IDSEL:AD22



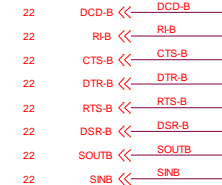
COM



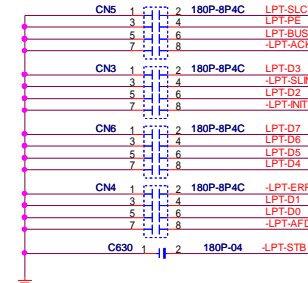
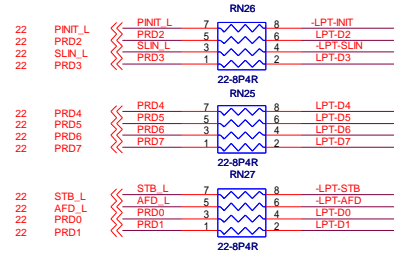
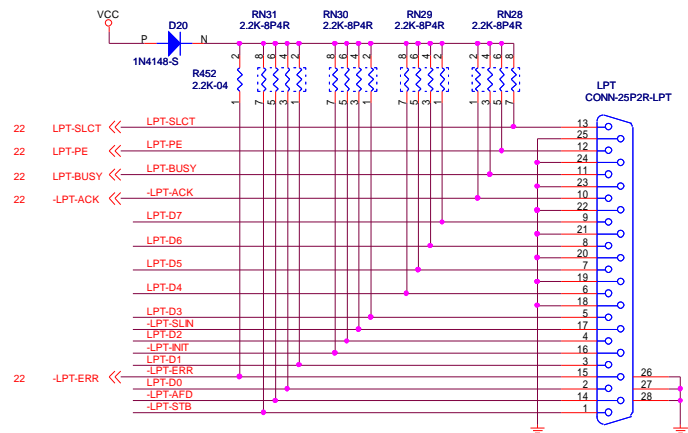
COM1 Port



COM2 Port

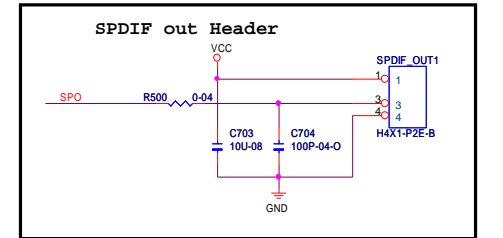
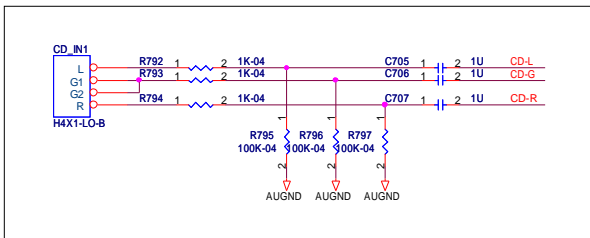
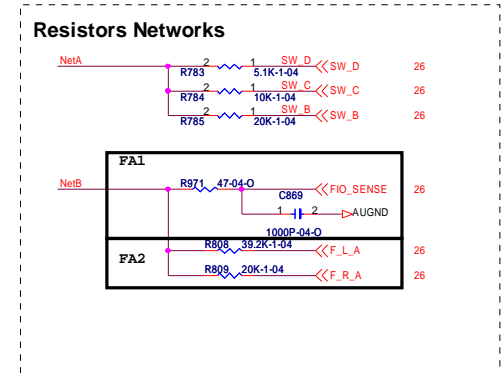
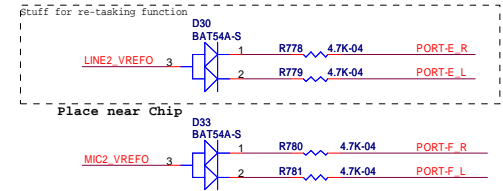
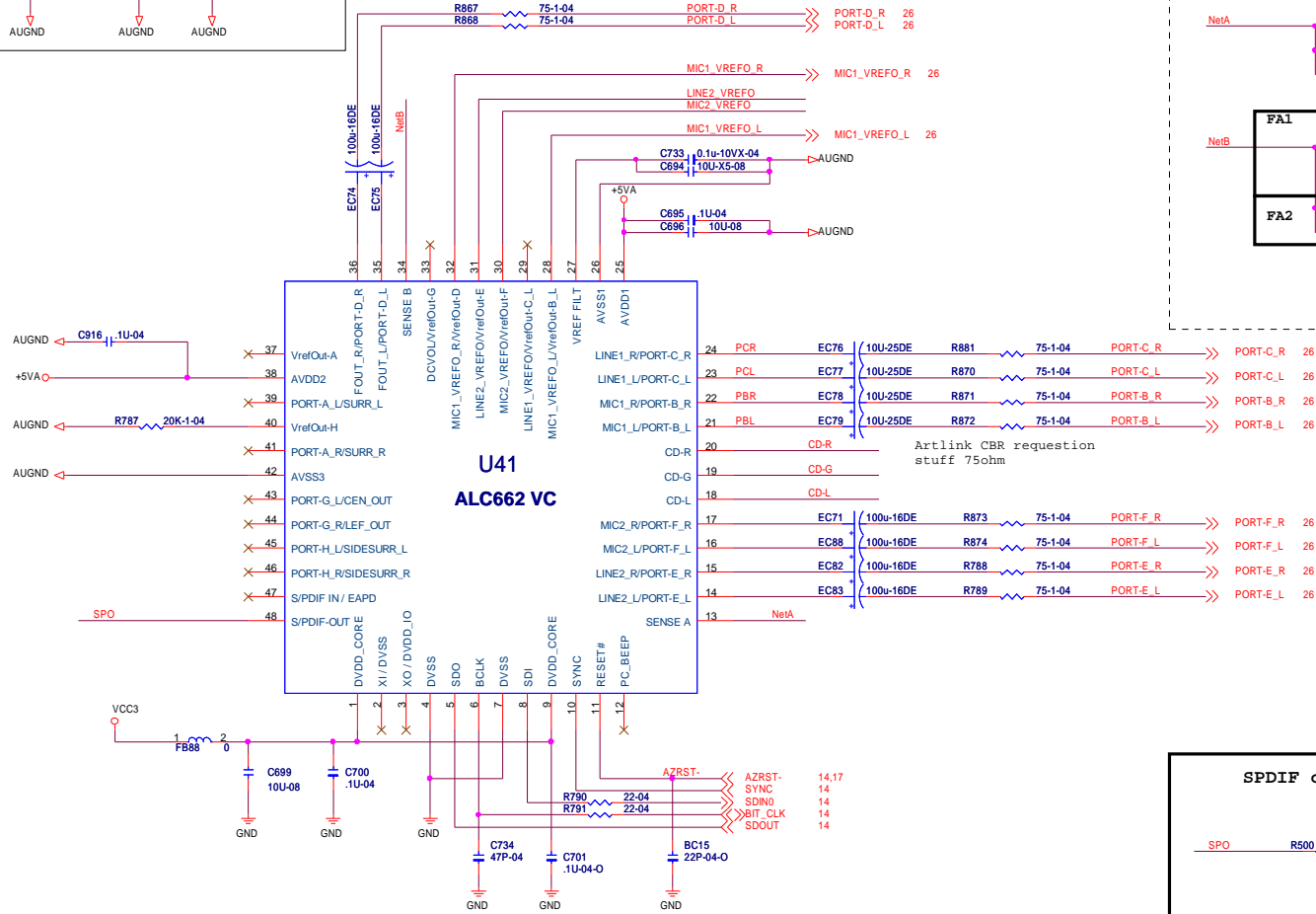
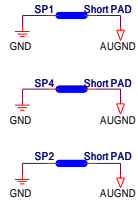
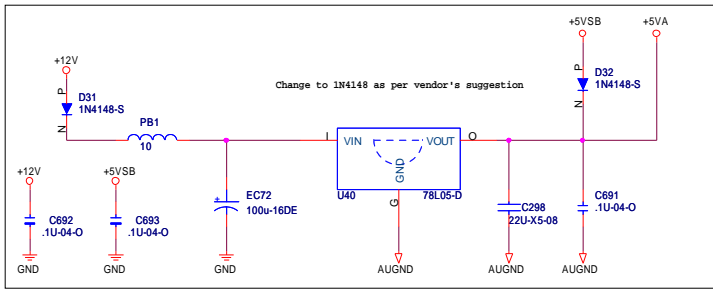


LPT



Elitegroup Computer Systems

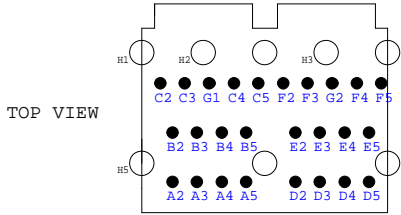
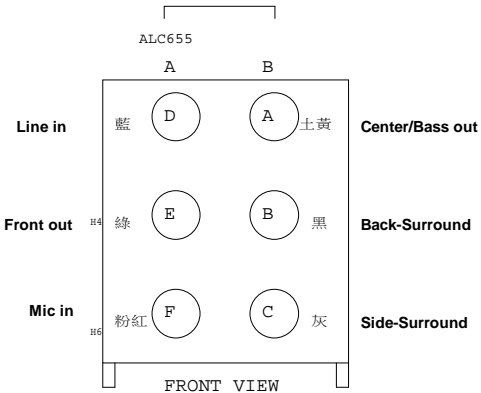
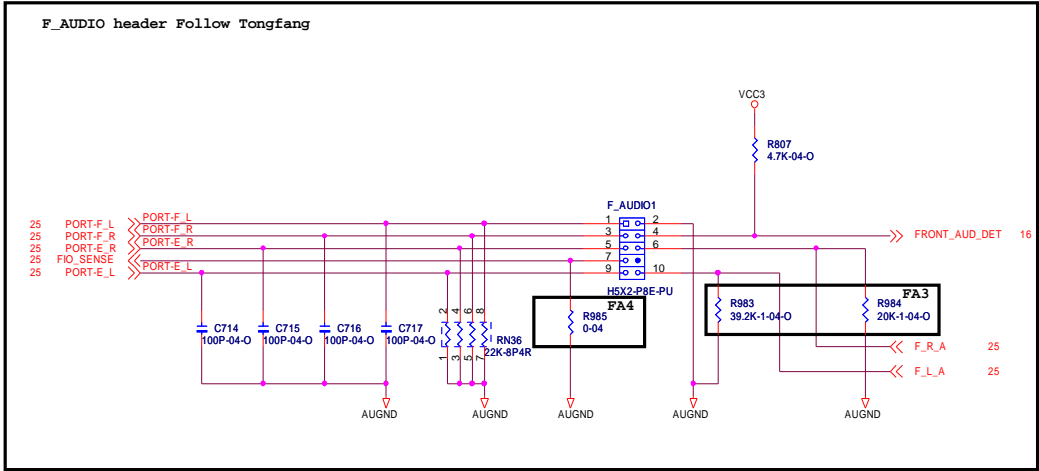
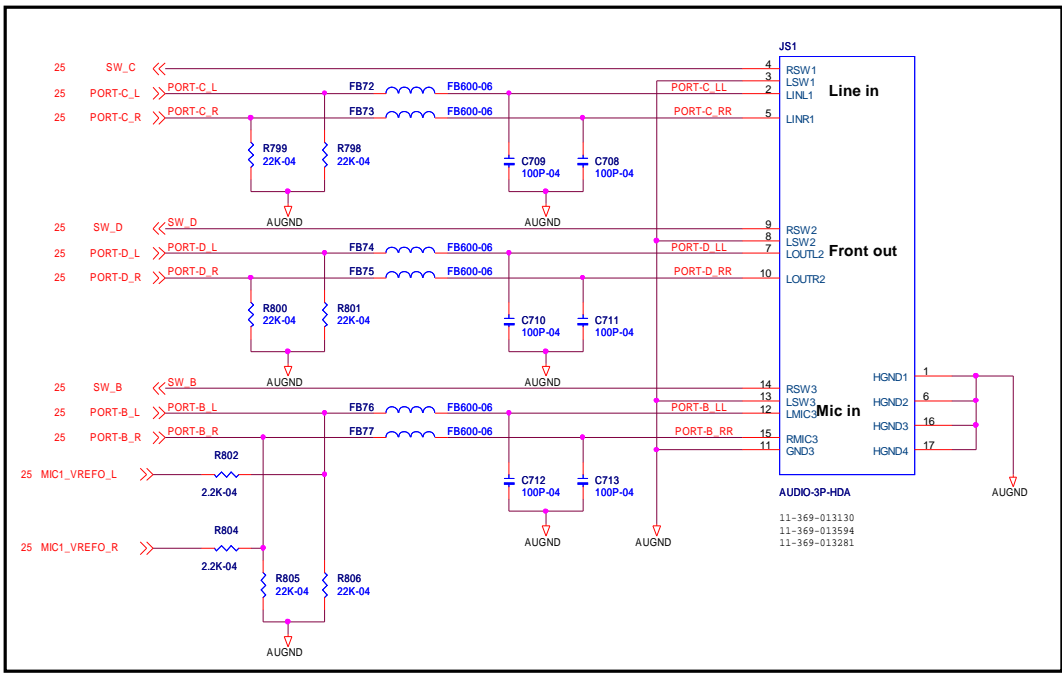
Title		
LPT/COM PORT		
RS780LQ-CM		
Size	Document Number	Rev
Custom		1.0
Date:	Tuesday, September 29, 2009	Sheet 23 of 32



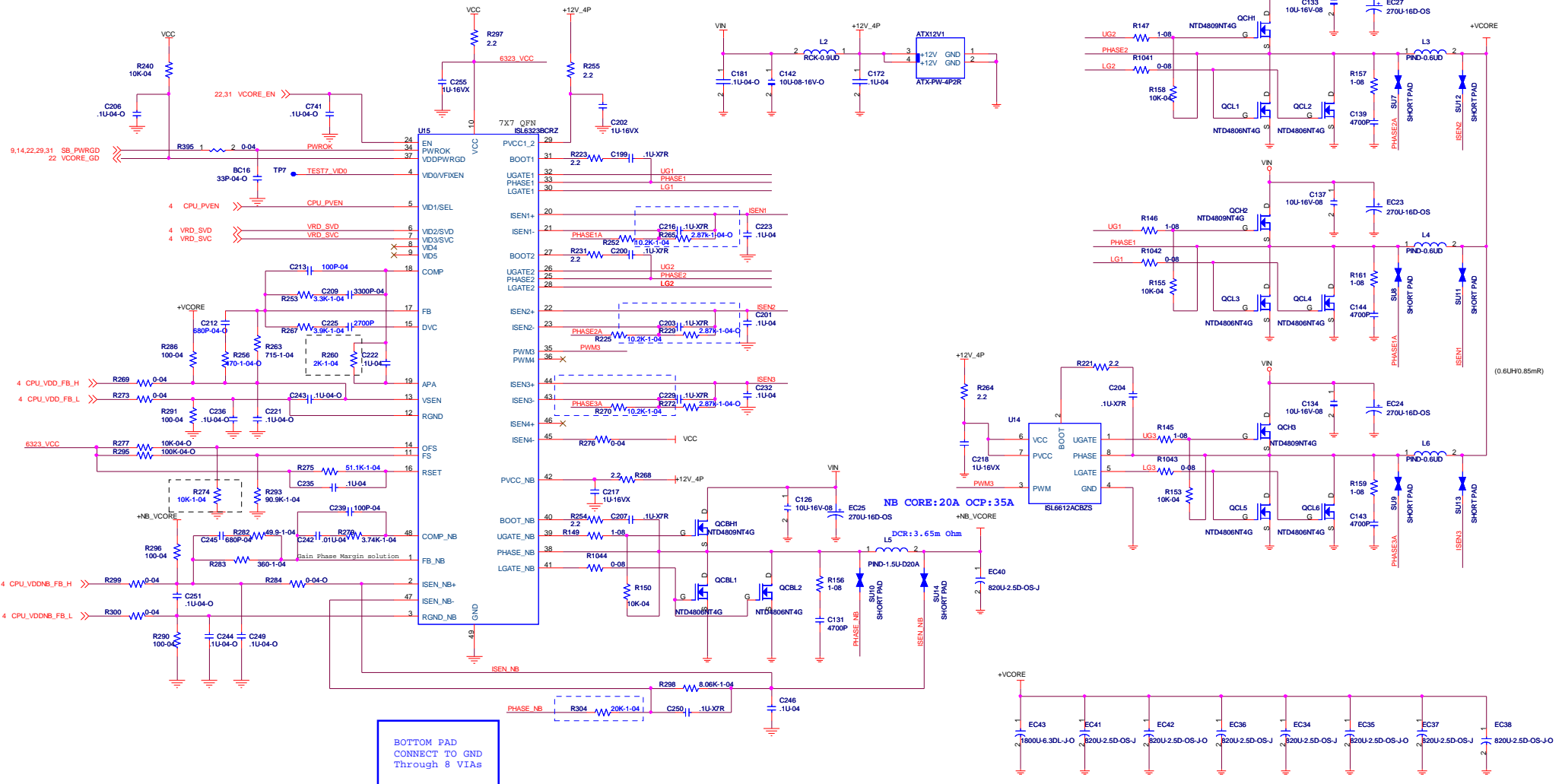
F_AUDIO	AC_97	HD Audio
FA1	STUFF	NC
FA2	NC	STUFF
FA3	STUFF	NC
FA4	NC	STUFF



Elitegroup Computer Systems

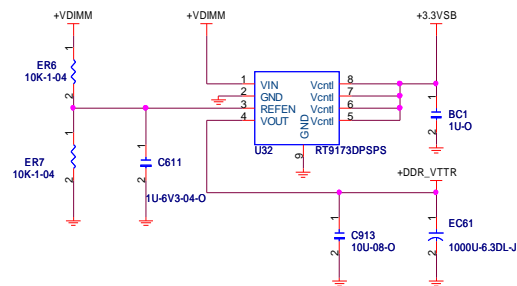


ISL6323CR CKT for Hybrid



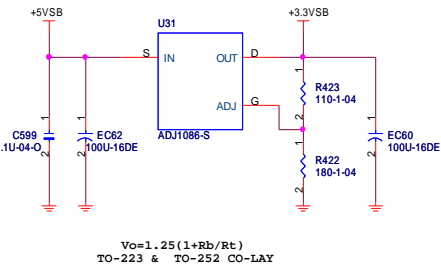
DDRVTT

0.9A



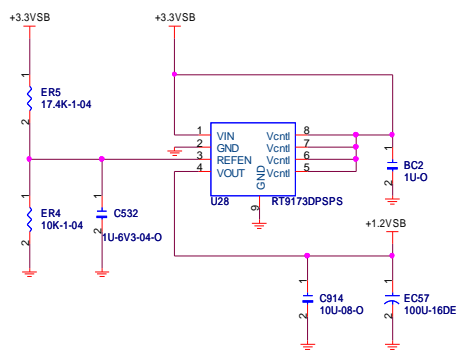
3VSB

1A



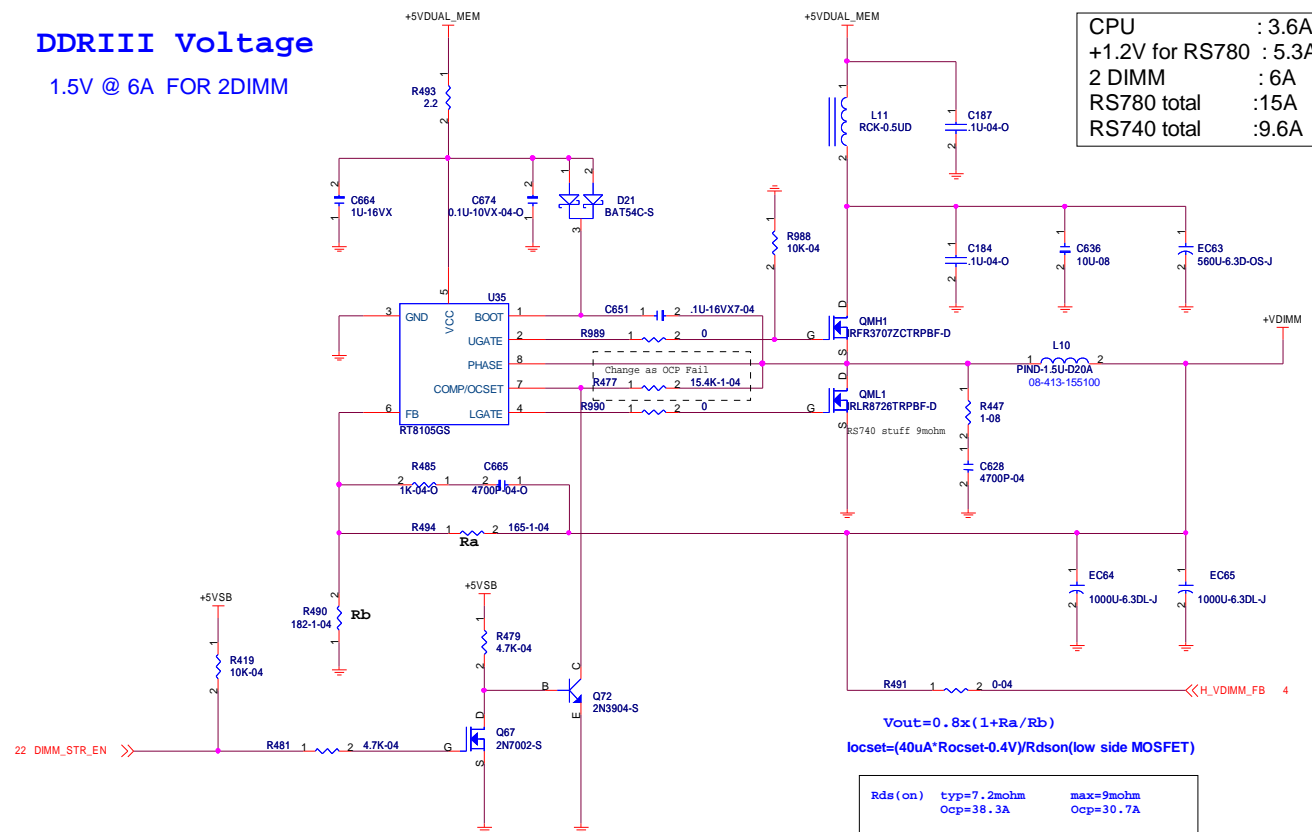
1.2 VSB

0.22A



DDRIII Voltage

1.5V @ 6A FOR 2DIMM



RS780 USE

80 USE

NB Core

[illegible]

SB_PWRGOOD Sequence

RS780 USE

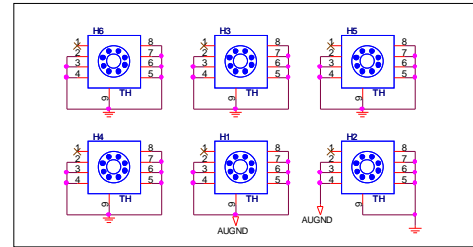
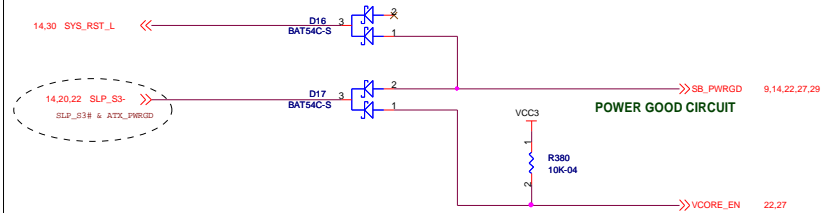
+12V EN
 VREF25
 R737 10.5K-1-04 RS780 Stuff
 C671 .1U-X7R RS780 Stuff
 R738 10K-1-04 RS780 Stuff
 U268 OP358-S RS780 & RS740 Stuff
 C753 .1U-04-0
 R866 1K-04-0
 Q71 IRLR8726TRPBF-D RS780 Stuff
 +HT 1P2V
 +VDIMM
 C672 .1U-X7R RS780 Stuff
 EC33 1000U-6.3DL-J
 NB_VCC
 R18 1 2 0-08-O StUFF for RS740
 R890 1 2 0-08-O StUFF for RS740
 R876 1 2 0-08-O StUFF for RS740

[illegible]

Elitegroup Computer Systems

Title				NB CORE POWER			
Size	Custom	Document Number				Rev	
		RS780LQ-CM				1.0	
Date:	Tuesday, September 29, 2009			Sheet	29	of	32

POWER GOOD & ENABLES



Elitegroup Computer Systems

Title

POWER ENABLE

Size
Custom

Document Number

RS780LQ-CM

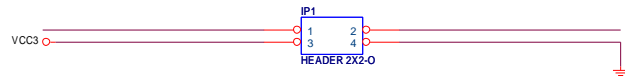
Rev
1.0

Date: Tuesday, September 29, 2009 Sheet 31 of 32

NOTE:若為LAYOUT方便可改為兩個1X2 HEADER

不上件

CUPON



2116 : trace width 5 mil 60 ohm
Trace Length 6096 mils
Spacing: 1.clearance to itself 20/5/20(S:W:S)
2.clearance to other signal 3W

1080 : trace width 4 mil 50 ohm
Trace Length 6096 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W

For 103

X2(wire)



XTAL-JW

For 104

SPI_ROM_D1(104)



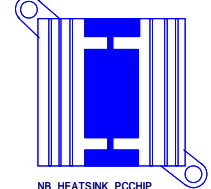
SPI-ROM-D-8M

BT1(104)



BATTERY

RS780(104)



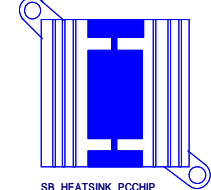
NB_HEATSINK_PCCHIP

CLR_CMOS1(104)



JP-R-H

SB700(104)1



SB_HEATSINK_PCCHIP



Elitegroup Computer Systems

Title

Attention

Size

Custom Document Number

RS780LQ-CM

Rev

1.0

Date: Tuesday, September 29, 2009

Sheet 32 of 32